REMARKS

The Final Action dated March 17, 2006 in this Application has been carefully considered. Claims 1-10, 12-14, 16, 18, 19, 21-23 are pending. The above requested amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claim 8 has been amended in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

Claim 8 has been amended in this Response to correct a minor typographical error. Accordingly, Applicants respectfully request that the Examiner enter the amendment of Claim 8 as it places the Claims in better condition for appeal.

Claims 1-6, 8-10, 12-14, 18-19, and 21 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 6,430,656 by Arimilli et al. ("Ar'656") in view of U.S. Patent No. 6,145,057 by Arimilli et al. ("Ar'057"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claim 1, Ar'656 was cited as assertedly fully disclosing, among other things:

(1) "a range register coupled to receive an address and configured to produce" (*citing* Ar'656, col. 4, lines 22-66; Fig. 2, #11);

(2) "(i) the class identifier corresponding to the memory region having an address range that includes the received address" (*citing* Ar'656, col. 6; Fig. 2, #16); and

(3) "(ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address." Final Action, at Page 3.

The Examiner admits that Ar'656 "does not describes the tag replacement control indicia." Final Action, at Page 4. To supply this missing element (and a number of other elements), the Examiner offers Ar'057, stating that "It would have been obvious to one of ordinary skill in the art

at the time of invention to include the LRU logic and indication signals as suggested by Ar'057 in Arimilli'656's thereby allowing quick resolve of replacement for cache entries in response to multiple requests in a multiprocessor data processing system." Final Action, at Page 4.

The Examiner's proposed combination fails for a number of reasons.

First, Ar'656 does not in fact teach "a range register coupled to receive an address and configured to produce (i) the class identifier corresponding to the memory region having an address range that includes the received address or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address" as recited in Claim 1 and as alleged by the Examiner. Second, Ar'057 likewise fails to teach tag replacement control indicia as alleged by the Examiner. Finally, there is no motivation to combine Ar'656 with Ar'057 to produce the claimed invention, and even if such motivation existed, which is does not, the proposed combination fails to teach each and every element as claimed.

The Examiner alleges that Ar'656 teaches "a range register" with certain functionality as claimed. Instead, Ar'656 teaches "an address 11" which includes, among other things, an "address field 13" and a "lower portion 14." *See* Ar'656, col. 4, lines 36-39. Applicants respectfully submit that, clearly, a mere "address" cannot be said to constitute a specific register that performs certain particular functions. That is, an "address" does not show "a range register coupled to receive an address and configured to produce (i) the class identifier corresponding to the memory region having an address range that includes the received address or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address" as recited in Claim 1. For at least this reason the Examiner's proposed combination fails.

Next, the Examiner also alleges that Ar'057 shows the "tag replacement control indicia" as claimed. Here, too, the Examiner's proposed combination fails. The Examiner offers Ar'057 as

showing "a congruence cache directory that have the LRU logic and LRU indication associated with each entry of each congruence class." Final Action, at Page 4 (*citing* Ar'057, col. 3, lines 33-50; Fig. 2, #40). But the cited element of Ar'057 does not show "tag replacement control indicia" as claimed. Instead, the LRU logic of Ar'057 "stores an indication of how recently each entry within each congruence class of cache data 18 has been accessed." Ar'057, col. 3, lines 41-43. This cannot be said to be "tag replacement control indicia," as recited in the Claims.

Moreover, Ar'656 introduces an additional restriction that teaches away from "tag replacement control indicia": "in order to maintain critical blocks pinned in [the partition], the other blocks in excess of the associativity [sic] number that are mapped to [the partition] *should be unused*." Ar'656, col. 5, line 66 to col. 6, line 1 (emphasis added). These blocks are kept unused, otherwise, "the loading of values from the other blocks may cause the values from the pinned block to be overwritten (victimized and flushed from the cache)." Ar'656, col. 6, lines 1-4. Thus, Ar'656 modifies how physical pages are mapped to real addresses, through manipulation of the effective use of parts of congruency classes. As such, Ar'656 is not concerned with cache replacement control *per se*, and therefore not only does not disclose, but also actively teaches away from "tag replacement control indicia" as recited in the Claims.

Accordingly, there is no motivation to supply the particular congruence class configurations of Ar'656 with the system of Ar'057, as the proposed combination completely fails to teach the elements as recited in the Claims. That is, even if there were some purpose to combining Ar'656 with Ar'057, which Applicants do not concede, the combination fails to teach each and every element as Claimed. For at least this reason, the Examiner's proposed combination fails.

Claim 8 also recites similar distinguishing characteristics of the present invention as Claim 1, namely, "using the address to produce: (i) the class identifier corresponding to the memory region

having an address range that includes the received address, or (ii) a default class identifier in the event that none of the memory regions has an address range that includes the received address;" "using the produced class identifier to create a tag replacement control indicia through employment of a replacement management table, wherein the tag replacement control indicia is indicative of the sets of the cache that may be used to store data retrieved from one of the memory regions having the produced class identifier;" and "configuring the replacement eligibility of the at least one set in the cache as a function of the tag replacement control indicia." For at least the forgoing reasons, the Examiner's proposed combination likewise fails to teach each and every element of Claim 8.

Claims 18 and 21 recite similar limitations as Claims 1 and 8. As such, the Examiner's proposed combination likewise fails to teach each and every element of Claims 18 and 21.

In view of the foregoing, it is apparent that the cited references do not disclose, teach or suggest the unique combinations recited in Claims 1, 8, 18, and 21. Applicants therefore submit that Claims 1, 8, 18, and 21 are clearly and precisely distinguishable over the cited references in a patentable sense, and are therefore allowable over these references and the remaining references of record. Accordingly, Applicants respectfully request that Claims 1, 8, 18, and 21 be allowed.

Claims 2-7 depend on and further limit Claim 1. Claims 9-10, 12-14, and 16 depend on and further limit Claim 8. Claim 19 depends on and further limits Claim 18. Claims 22-23 depend on and further limit Claim 21. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that dependent Claims 2-7, 9-10, 12-14, 16, 19, and 22-23 also be allowed.

Claims 16 and 22 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ar'656 and Ar'057 and further in view of U.S. Patent No. 5,974,507 by Arimilli et al. ("Ar'507"). Applicants respectfully traverse these rejections. In particular, Applicants submit that

Claims 16 and 22 are patentable over the Examiner's proposed combination for at least the reasons that Claims 1, 8, and 21 are patentable. That is, the combination of Ar'656 and Ar'057 fails to teach each and every element of the independent Claims 8 and 21, from which Claims 16 and 21 depend, as described above. For at least this reason, Applicants respectfully request that the rejections against Claims 16 and 22 be withdrawn and that Claims 16 and 22 be allowed.

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ar'656 and Ar'057 and further in view of U.S. Patent No. 5,708,789 by McClure et al. ("McClure"). Applicants respectfully traverse this rejection. In particular, Applicants submit that Claim 23 is patentable over the Examiner's proposed combination for at least the reasons that Claims 1, 8, and 21 are patentable. That is, the combination of Ar'656 and Ar'057 fails to teach each and every element of independent Claim 21, from which Claim 23 depends, as described above. For at least this reason, Applicants respectfully request that the rejection against Claim 23 be withdrawn and that Claim 23 be allowed.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Ar'656 and Ar'057 and further in view of U.S. Patent No. 6,826,652 by Chauvel et al. ("Chauvel"). Applicants respectfully traverse this rejection. In particular, Applicants submit that Claim 7 is patentable over the Examiner's proposed combination for at least the reasons that Claims 1 and 8 are patentable. That is, the combination of Ar'656 and Ar'057 fails to teach each and every element of independent Claim 1, from which Claim 7 depends, as described above. For at least this reason, Applicants respectfully request that the rejection against Claim 7 be withdrawn and that Claim 7 be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-10, 12-14, 16, 18, 19, 21-23.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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